AMENDMENTS TO CLAIMS

1. **(currently amended)** A buffer control apparatus in a buffered switch for controlling transmission of data, comprising:
a buffer memory for storing the data;
a buffer write module for writing the data into the buffer memory;
a buffer read module for reading the data from the buffer memory;
a deferred header queue containing entries having destination and buffer address information for data to be deferred, with entries for data addressed to multiple destinations ports being intermingled within the deferred header queue;
a header select device for controlling the buffer read module and having an initial and a deferred state,
the initial state adding entries to the deferred queue so as to temporarily defer transmission to a destination port unavailable to receive the data, and
the deferred state processing all entries in the deferred header queue in the order in which the entries were written in the deferred header queue, the deferred state submitting the buffer address information for an entry to the buffer read module when the destination port is available to receive data or the deferred state keeping the buffer address information on the deferred header queue when the destination port is unavailable to receive data.

2-3. **(cancelled)**

4. **(previously presented)** The buffer control apparatus according to claim 1, wherein the header select device further has a backup state wherein data received during the deferred state is analyzed for transmission or deferral after the deferred state has reviewed all entries in the deferred header queue.

5. **(previously presented)** The buffer control apparatus according to claim 4, further comprising:
a backup header queue containing entries for data that during the deferred state.

6. **(cancelled)**

7. (**previously presented**) The buffer control apparatus according to claim 1, wherein an XOFF mask is used to determine the current status of all destination ports in the buffered switch, the XOFF mask being a memory device having a bit associated with each possible destination ports, with each bit indicating either the ability or inability of the destination port to receive data.

8. (**currently amended**) The buffer control apparatus according to claim 1, wherein [[the]] each deferred header queue ~~entries each~~ entry comprises header information for a data frame and a starting address in the buffer memory for the data frame.

9. (**currently amended**) The buffer control apparatus according to claim 5, wherein ~~the~~ each backup header queue ~~entries each~~ entry comprises header information for a data frame and a starting address in the buffer memory for the data frame.

10. (**currently amended**) A deferred queue device for temporarily deferring transmission of packets/frames to a destination port in a buffered switch, comprising:

a deferred header queue device for storing frame information for packets/frames being deferred, the deferred header queue device containing information for packets/frames addressed to more than one destination port;

means for periodically determining current status of all destination ports in the buffered switch; and

header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame which can now be sent to an available destination port.

11. (**currently amended**) The deferred queue device according to claim 10, wherein the deferred queue device further comprises a state engine that can be in one of an Initial State, a Deferred State, and a Backup State.

12. (**original**) The deferred queue device according to claim 10, further comprising: a backup header queue device for storing frame information for packets/frames waiting to be sent to at least one destination port because the packets/frames arrived at an input port while deferred packets/frames were being sent to the at least one destination port.

13. (**currently amended**) The deferred queue device according to claim 10, further comprising: a backup header queue device that operates in parallel with the

deferred header queue device for storing frame information for packets/frames waiting to be sent to at least one destination port.

14. (**previously presented**) The deferred queue device according to claim 10, wherein an XOFF mask is used to determine the current status of all destination ports in the buffered switch, the XOFF mask being a memory device having a bit associated with each possible destination ports, with each bit indicating either the ability or inability of the destination port to receive data.

15. (**cancelled**)

16. (**currently amended**) The ~~buffer control apparatus~~ deferred queue device according to claim 10, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

17. (**currently amended**) The ~~buffer control apparatus~~ deferred queue device according to claim 12, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

18. (**currently amended**) A method for temporarily deferring transmission of data to a destination port in a buffered switch, comprising the steps of:

    a. during an initial state:

        i. receiving a request for transmission of data to the destination port;

        ii. determining whether the destination port is available to receive the data;

        iii. deferring transmission of the data when the determining step determines that the destination port is not available to receive the data by storing entries including destinations for the data to be deferred in a deferred header queue ~~whereby~~ simultaneously containing entries corresponding to data addressed to different destination ports ~~are simultaneously stored in the same deferred queue~~;

        iv. transmitting data to the destination port when the determining step determines the destination port is available to receive the data; and

        v. repeating the above steps i-iv for all data to be transmitted.

b. upon receiving notification that a destination port has changed state and may now receive data, entering into a deferred state during which:

i. all entries in the deferred header queue are analyzed in the order in which the entries ~~are~~ were added to the deferred header queue;

ii. upon determining that the destination port for ~~a data~~ an entry in the deferred header queue is now able to receive data, transmitting the corresponding deferred data to the destination port;

iii. upon determining the destination port for ~~a data~~ an entry in the deferred header queue is still not able to receive data, ensuring the entry corresponding to the data remains in the deferred header queue; and

iv. repeating steps i-iii for all entries in the deferred header queue.

19-22. (**cancelled**)

23. (**currently amended**) The method according to claim 18, further comprising the steps of: storing in a backup header queue entries including destinations for data received during the deferred state; and further comprising the steps of:

c. upon completing step b, entering a backup state whenever there is data having at least one entry in the backup header queue by performing the steps of:

i. periodically checking to determine if the destination ports for data having entries in the backup header queue are available;

ii. transmitting the data to the destination ports when it is determined that the destination ports are available;

iii. placing entries including destinations for the data [[in]]into the deferred header queue when it is determined that the destination ports are not available.

24. (**currently amended**) The method according to claim 23, wherein the data is transmitted to the destination port in the order in which entries for the data ~~was~~ were received at the backup header queue for the destination port.

25. (**currently amended**) The method of claim 18, wherein entries in the deferred header queue ~~comprises a header queue containing header information for all data in the queue, the header information containing destination information~~

~~and~~ further include a buffer address location indicating where the data resides in a buffer memory.

26. (**currently amended**) A data switch having a plurality of output ports, each output port having a positive or negative transmission status; the switch comprising:

a. an input buffer receiving a plurality of data frames each associated with ~~anoutput~~ an output port;

b. a mechanism at each input buffer to determine the transmission status of the output ports;

c. a deferred header queue in which destination entries for data for a plurality of different output ports having a negative transmission status [[is]]are tracked;

d. a backup header queue in which destination entries for newly received data [[is]]are queued when [[data]]destination entries in the deferred header queue [[is]]are being processed; and

e. a state machine that enters a deferred state when an output port moves from a negative to a positive transmission status, the deferred state causing the data switch:

i. to process [[data]]destination entries in the deferred header queue so as to transmit to the associated output port that data which is addressed to an output port that now has a positive transmission status,

ii. to ensure that [[data]]destination entries in the deferred header queue addressed to output ports that still have a negative transmission status remain in the deferred header queue, and

iii. to place destination entries for newly received data in the backup header queue.

27. (**currently amended**) The data switch of claim 26, wherein the state machine enters a backup state when all [[data]]destination entries in the deferred header queue [[is]]are processed in the deferred state and [[data]]destination entries exists in the backup header queue, the backup state causing the data switch to determine whether the data corresponding to destination entries in the backup header queue should be transmitted to its associated output ports or the

destination entries should be stored in the deferred header queue based upon the transmission status of the data's associated output port.

28. (**previously presented**) The data switch of claim 27, wherein the state machine moves from the backup state to the deferred state when an output port moves from the negative transmission state to the positive transmission status.

29. (**currently amended**) The data switch of claim 28, wherein the state machine enters a normal state when the deferred state is completed and no ~~data exists~~ destination entries exist in the backup header queue, or when the backup state is completed and no port has moved from the negative transmission state to the positive transmission state, and wherein the normal state causes the data switch to determine whether incoming data should be transmitted to the associated output port or destination entries corresponding to the incoming data be queued on the deferred queue depending on the transmission status of the associated output port.

30. (**previously presented**) The data switch of claim 26, wherein the mechanisms to determine the transmission status of the output ports is an XOFF mask.

31. (**previously presented**) The data switch of claim 30, wherein the XOFF mask comprises a memory device having a bit associated with every output port, with each bit indicating either the ability or inability of the output port to receive data at a current time.

32. (**currently amended**) The data switch of claim 30, wherein the XOFF mask is updated in real time except during the deferred state, during which time changes to the XOFF mask indicating a change of a port transmission status from negative to positive are delayed until all destination entries in the deferred queue have been analyzed.

33. (**currently amended**) The data switch of claim 32, wherein the deferred state is reentered with an updated XOFF mask after all destination entries in the deferred queue are analyzed with an original XOFF mask if the change of a port transmission status from negative to positive occurs during the deferred state.

34. (**previously presented**) The data switch of claim 26, wherein the data frames are selected from a group of frames comprising fixed length frames and packets, frames and packets having end of frame delimiters, and variable length data frames and packets.

35. (**currently amended**) A data switch having a plurality of destination ports comprising:

a deferred header queue that stores destination entries for data being deferred,

the deferred header queue [[means]] containing entries for data addressed to more than one destination port; and

a logic unit having an initial state and a deferred state,

in the initial state the logic unit transmits data to non-blocked destination ports and adds destination entries for data to the deferred header queue where that data is addressed to a blocked destination port, and

in the deferred state the logic unit processes [[data]]destination entries in the deferred header queue by transmitting to its destination port [[that]] the corresponding deferred data that is addressed to a no longer blocked destination port, and by retaining within the deferred header queue destination entries for data that [[is]]are addressed to [[a]] still-blocked destination [[port]]ports.

36. (**new**) An apparatus for handling head-of-line blocking in a buffered switch in which two switch output ports that have been blocked, comprising a deferred header queue containing intermingled entries for deferred data destined to the two output ports, each entry including the port to which the corresponding data is destined.

37. (**new**) The apparatus of claim 36, wherein each entry further includes an address of the data in an input buffer.